

80Gb/s Multi-Level BPSK experiment with an InP-Monolithic Source Based on Prefixed Optical Phase Switching

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Short-Abstract — Improved-speed full-monolithic BPSK transmitter based on prefixed phase switching by fast Electro-Absorption Modulators has been realized on InP using a Selective Area Growth integrating circuit technology. It has been used in 80Gb/s multi-level BPSK format modulation experiments. Simplicity, speed scalability, ultra-small footprint and low power drive of the monolithic circuit are attractive for advanced format migration towards low-cost applications.

I. INTRODUCTION

Increasing component speed, throughput and efficiency inevitably leads to optoelectronic transmitters and receivers of more complexity, larger footprint, consumption and cost. Monolithic integration is known to help solving these problems typical of discrete components. However, cost, consumption and material usage lowering must preserve high modulation performance specially while increasing the data rate.

Monolithic integration on InP is a way to facilitate the design of complex photonic circuits with multiple photonic functions. Previously inspired from LiNbO₃ architectures, they showed issues with a large footprint, important optical losses, high power consumption and integration compatibility with a laser [1]. A novel, very simple way, to generate the advanced formats has been proposed by Inuk Kang who used short Electro-Absorption Modulators (EAM) in an interferometric arrangement [2]. Low power consumption EAMs acting as a prefixed optical phase switch were shown to simplify and reduce the circuit size. We previously demonstrated 12.5Gb/s [3] and then 28Gb/s [4] BPSK modulation ability of first full-monolithic transmitters chips integrating on InP a DFB laser emitting at 1.550 μm and a 2-arms interferometer based on the EAM phase switching.

In this work we report on speed improvement of the circuit and on its ability to generate multi-level modulation formats. The Photonic Integrated Circuit (PIC) has been fabricated using a relatively simple technology based on a single active layer growth composed of AlGaInAs quantum wells, Selective Area Growth (SAG) gap engineering and a single regrowth semi-insulating buried hetero-structure (SIBH) [5].

The integrated monolithic transmitter has been used in 80 Gb/s (2x40 GB) multi-level BPSK. This new spectrally

efficient format uses two phase states 0 and π and m (here $m=4$) amplitude ones (ex. -1, -0.5, 0.5, 1). While keeping simple the transmitter and its driving electronics, it has an advantage over more standard m -ASK (or m -Pulse AM) to suppress the optical carrier and, therefore, to provide a better energy efficiency and a lower transmission penalty.

II. DEVICE CONCEPT, TECHNOLOGY AND CHARACTERISTICS

The BPSK TX PIC operation principle relies on two-arm interferometric waveguide arrangement with optical phases $0-\pi$ prefixed by 1:2 MMI power splitter and DC-current controlled phase shifters. EAM in each arm switches on/off appropriate phase reflecting a modulation data (Fig 1). The waveguides are then combined in 2:1 MMI into a single output. Interestingly, EAM switch is suitable to provide multiple power levels easily enabling simple spectrally-efficient multi-level BPSK formats. Full circuit dimensions are 2.65 mm x 0.5 mm remaining probably the smallest reported BPSK transmitter.

In order to simplify the fabrication and target its high yield, we choose a Selective Area Growth (SAG) for bandgap engineering of our circuit integrating passive and 3 different active regions made of AlGaInAs MQWs. In SAG, different areas of material optimized for active or passive optical function are defined in single epitaxial step by use of dielectric masks that locally enhance growth rate. Unlike the Butt-joint technique, self-aligned and genuinely continuous SAG guide avoids reflection between each area whatever was the number of engineered bandgaps. Fig 1 shows the simulated photoluminescence wavelength for each photonic function area of the BPSK chip.

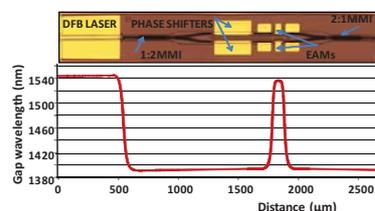


Fig 1. SAG design of photoluminescence wavelength for each photonic function area of the BPSK transmitter

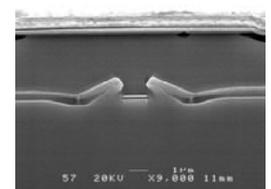


Fig 2. SEM view of a cross section of a semi-insulating buried heterostructure

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Second epitaxial technique used in the realization process of the component is the Semi Insulating Buried Heterostructure (SI-BH) for low RC product Electro-Absorption Modulators (EAM). In addition to its simplicity (only one single regrowth for all PIC components), it enhances the chip robustness, thermal dissipation and current confinement. A cross-view of a SI buried ridge is shown on Fig 2. A blocking layer prevents the inter-diffusion between the semi insulating InP and the upper p-doped InP which finishes to bury all the structure. The final device was coated with a high reflection (HR) coating on the laser side and with an anti-reflection (AR) coating on the output guide. The maximum output power the PIC observed for constructive interference state and unbiased EAMs reached +5 dBm at 150 mA leading to a coupled power above +2 dBm. The extinction ratio between constructive (0, 0) and destructive (0, π) interference states was above 20dB attesting good power balance and phase precision in the circuit arms [3]. In order to improve the component bandwidth we used 50 μ m EAMs [5]. Measured S21 and S11 are shown in Fig 3. The bandwidth is far above 26GHz, our measurement limit.

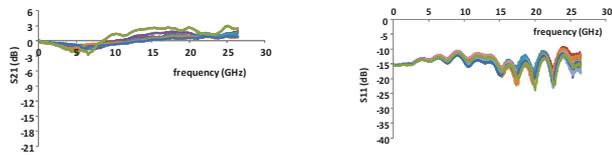


Fig 3. Frequency response S21(left) and S11(right) of 4 different BPSK TXs

III. MODULATION EXPERIMENTS

On-chip experimental bench was composed of 64bit PRBS generator, home-made flexible (1 or 2bit) InP-DAC (Digital-to-Analog-Converter) and signal amplifier generating data and inverted data modulation with 1.5Vpp NRZ or 2Vpp 4-level signals. As a receiver we used Optical Complex Spectrum Analyzer AP2443B from APEX (Fig 4). The data rate 40GB we used was limited by the available signal amplifier. 64 bit PRBS was made to correspond to a maximum sequence length analyzed by AP2443B [6].

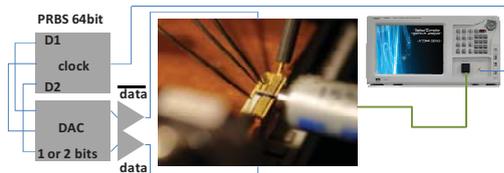


Fig 4. Experiment schematic with actual photography of the BPSK TX chip

First, we configured our DAC to generate 40 Gb/s 2-level 1.5 Vpp output. The BPSK circuit was designed to naturally provide 0, π phase states and only 0.2 mA on one phase shifter was applied for phase adjustment. As shown in Fig 5 DER>9dB (power and tributary eyes) has been obtained with this low power drive. The transitions between phase states showed a very small deviation from constellation horizontal I-axis attesting of a small EAM chirp influence on the signal.

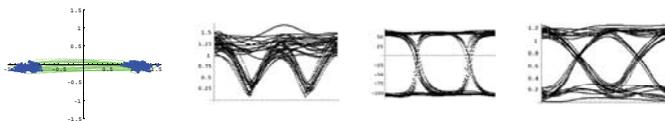


Fig 5. 40Gb/s BPSK acquired signal analysis (from left to right): constellation with transitions, power, phase and tributary eyes

In a next step we configured our DAC to provide 80Gb/s 4-level (2bit) 2Vpp output. Received signal with two-phase and multiple power states are shown in Fig 6. In spite of only 64-period analysis the constellation shows 4 distinguished power states and the absence of optical carrier due to BPSK format. Again, all transitions between phase/amplitude states are aligned along I-axis confirming low-chirp EAM switching. This property is similar to that observed for bulky push-pull Mach-Zehnder modulators. The tributary eye shows also well separated 4-levels.

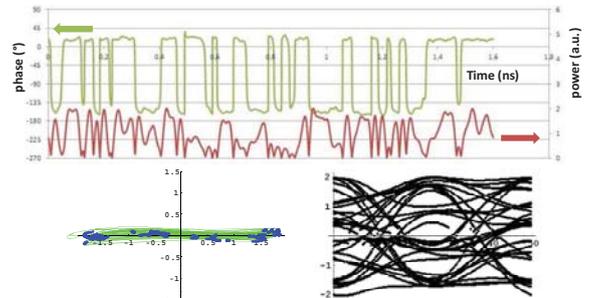


Fig 6. Multi-level BPSK phase and power sequence (upper), constellation with transitions and tributary eye (lower) of the generated 80Gb/s signal

IV. CONCLUSION

We fabricated a full-monolithic BPSK transmitter source based on prefixed phase switching by fast EAMs using a SAG photonic integrating circuit technology. This work demonstrates the smallest 80 Gb/s BPSK transmitter and confirms its ability to generate high-speed multi-level formats. Small package compatible footprint and low power drive of the EAM based integrated sources are attractive for advanced format migration towards ultra-fast low-cost applications.

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